Fused Silica based RSOL calibration substrate for improved probe-level calibration accuracy

Luca Galatro, Marco Spirito

Electronics Research Laboratory (ERL), Delft University of Technology, Delft, The Netherlands,

***Abstract* — In this contribution we present a calibration substrate manufactured with integrated circuit technology on fused silica, used for reciprocal SOL calibration. The fabrication technology is described together with the standard layout, and the precise control of the geometrical properties is exploited to create accurate pitch-dependent standard model to be used during the calibration procedure. The calibration accuracy is benchmarked with the conventional alumina impedance standard substrates, using the provided (polynomial fit) standard definitions, giving an estimate of the accuracy improvement that the proposed calibration substrate can provide.**

***Index Terms* — VNA, calibration, on-wafer, probe-level, RSOL, fused silica.**

I. Introduction

The accuracy of S-parameter measurements of any device under test (DUT) is set, at the first order, by the quality of the VNA calibration. This is typically performed by measuring a certain number of known devices (i.e., the calibration standards). Depending on the specific calibration technique employed, the quality of the calibration is directly dependent on the accuracy with which the calibration standards are known/modeled [1][2]. When considering planar devices, for which wafer-probes need to be employed, it is common practice to perform a probe-level calibration (first-tier) using a low-loss substrate (i.e., alumina or fused silica), which can then be transferred to the environment where the DUT is embedded. In planar environments, the accurate modeling of the calibration standards can become cumbersome, due to ambiguity in the definition of the calibration reference plane [3] and the limited control on the accuracy with which the standards are manufactured. For this reason, calibration techniques in which little knowledge of the standards is required, like TRL [4] and LRM [5], might be preferred. However, TRL calibration results to be impractical for probe level calibrations performed on general purpose substrates when a broadband range of frequencies is considered, due to the large number of long transmission lines that would be required. Also, both TRL and LRM calibration define the calibration reference plane at the center of the (non-zero) thru standard, and not at the probe tips. While moving the reference plane to the probe tips is possible by considering single mode propagation in the thru line, this assumption is generally violated in the close proximity of the probe tips, due to higher order modes generated at the non-ideal probe-to-line transition [6]. On the other end, SOL calibration using an unknown thru (RSOL [7]) has been proven to be as accurate as TRL calibration, when a sufficiently accurate model of the standards is provided [8]-[10]. Also in this case, as the authors described in [3] and [10], the calibration reference plane can be univocally defined using EM simulations for the standard modeling. This technique also allows to create probe-independent calibration kits, as opposed to the conventional probe-paired calibration substrates [11], where the imperfections of the probe-to-line transition are embedded in the DUT instead than in the calibration error terms, leading to measurement error [3].

In order to achieve accurate calibration standard modeling, additional care should be dedicated to the manufacturing of the calibration standards. The process presented in [10], based on integrated circuit technology, and the use of fused silica as substrate, had the goal of improving the quality of the standard manufacturing with a special focus on the load, in order to increase repeatability and avoid the common practice of resistance tuning via laser trimming.

In this contribution we present a RSOL calibration kit manufactured on fused silica with the process described in [10] and its performances, in terms of measurement accuracy, when employed for VNA calibration in the frequency range from 10 MHz to 50 GHz. The paper is structured as follows, first the process technique and the layout of the calibration kit are described. Then, the modeling of the calibration standards is discussed. Finally, the proposed calibration kit is used for VNA calibration and measurements of both one port and two ports passive devices are employed to compare it towards a commercially available alumina calibration kit.

II. Fabrication technology

For RSOL as well as for LRM calibration, the variation of the load performances, both in terms of DC resistance and electromagnetic behavior, constitute one of the biggest sources of uncertainty [9][10]. In commercially available calibration kits, the load standard is typically defined by means of a purely inductive model [12]. In this, while the DC resistance is very well controlled by means of laser trimming [11], the purely inductive model results to be inaccurate since the large capacitive loading provided by the contacting metal stripes is neglected [10]. At the same time, the laser trimming procedure, while keeping the resistance value highly repeatable, poses a limit in the EM modeling of the load

standard, since the geometrical modifications generated during the trimming procedure are not predictable. The only way to avoid laser trimming is to use a fabrication process that could allow very precise control of the geometrical properties (width/thickness) of the resistive layer. In this framework, a lithographic process like the one proposed in [10], featuring a layer thickness variation in the order of 1% across a single 2x2 cm^2 and horizontal accuracy in the order of parts of nanometer, can represent a good candidate for the manufacturing of a precision RSOL calibration substrate.

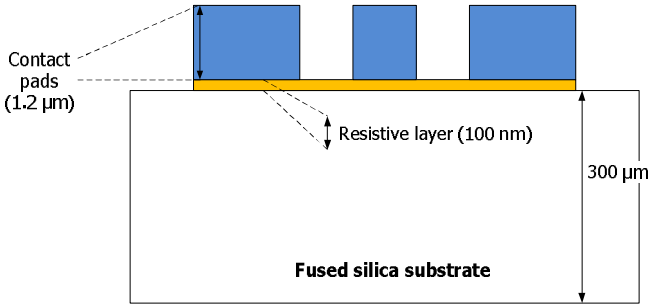


Fig. 1: Schematic cross section of the 50 Ω resistors fabricated on the proposed fused silica substrate

Fig. 1 shows a simplified schematic cross section of a calibration load manufactured in the proposed technology. The resistive layer with controlled thickness is first deposited, then patterned by means of lithography. The contact pads are then deposited on top of the resistive layers, in order to guarantee a good ohmic contact between the low resistivity material of the pad (aluminum) and the high resistivity material used for the resistance.

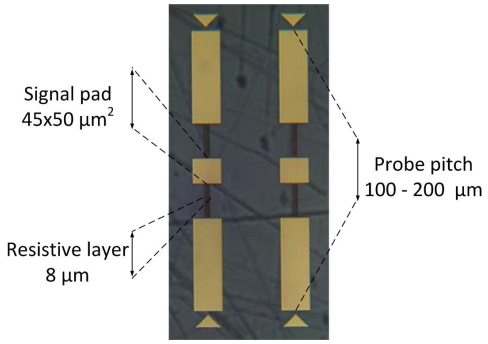


Fig. 2: Load standard artifact realized using the proposed technology

For the other standards (short, open and thru) the same manufacturing process is used, with the low resistivity material always deposited on top of the high resistivity layer. Fig. 2 shows one of the load artifact realized on the proposed technology. All the designed structures feature a 45x50 μm^2 signal pad, and a geometry which can allocate probe pitches in the range 100-200 µm.

III. Simulation Setup

In order to realize an accurate model for the calibration devices manufactured as described in section II, EM simulators have been employed. Being the structures mostly planar, a 2.5D full-wave EM environment (i.e., Keysight Momentum) can be considered of sufficient accuracy for the purpose. For each calibration standards, the material properties and geometrical characteristics (width and length) have been defined as provided by the manufacturer. The resistive layer thickness value has been extracted by means of DC measurements, using the width, length and resistivity as constants. The contact of wafer probes is simulated by means of internal ports, and different models have to be defined for different probe pitches, since the behavior of the standards is dependent on the distance between the stimuli. On the other hand, as described in [10], the impact of probe displacement on the wafer pads during an RSOL calibration is weak, for this reason the ports can be safely placed at the center (in the x direction) of the pads, i.e., at 25 µm from the border, without losing in generality, as depicted in Fig. 3a. The result is a pitch-dependent model, but no other probe effect needs to be taken into account, while the calibration reference plane will be only weakly sensitive on the probe positioning.

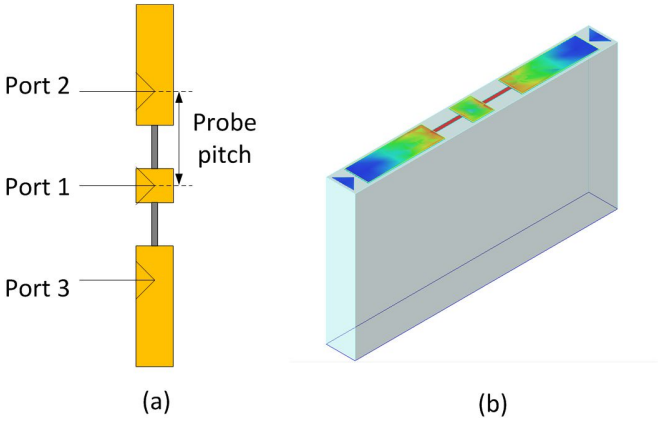


Fig. 3: a) Simulation setup in Keysight momentum for the load standard. The port positioning depends upon the targeted probe pitch. b) 3D model of the load standard after simulation, indicating field density over the conductor and resistive layer surface.

After the simulations, the S-parameters of each standard can be extracted, and then used as calibration standard model instead of using the probe-paired calibration coefficients.

IV. Experimental Results

Once the calibration kit is manufactured and properly modeled, the performances can be evaluated by means of comparison. In order to do that, measurements have been performed in the frequency range from 10 MHz to 50 GHz,

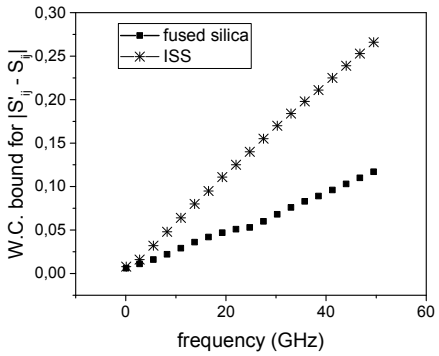
employing a set of Cascade Microtech Infinity i50 probes with 125 µm pitch, using Cascade Microtech Wincal XE ver. 4.5 for the data acquisition and calibration computation. First a RSOL calibration has been performed by using the calibration kit presented in section II in combination with the model realized as described in section III, and the error terms have been saved. Then another RSOL calibration has been conducted on a Cascade Microtech ISS model 101-190C [12], using manufacturer definitions for the standards. Finally, a unique set of raw measurements has been conducted on different DUTs: a set of different loads manufactured with the technology described in section II (0.35 Ω, 0.45 Ω, 41 Ω, 4500 Ω, 6800 Ω), two CPW lines realized on fused silica (726 µm, 1422 µm), a verification line from the ISS substrate (1800 µm) and a CPW line realized on SiGe BiCMOS 130nm technology (600 µm). The two different calibrations have been then applied to each one of the raw measurements. In order to compare the performance of the calibration, the method of [6] has been employed, using simulation data as reference, and defining two different worst case error bounds for the loads and for the transmission lines:

$$WC_{load} = \max\left|S^{k}_{ii,n} - S^{Ref_k}_{ii,n}\right| \quad (1)$$

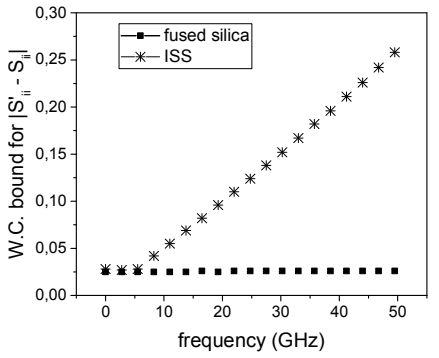
$$WC_{line} = \max\left|S^{w}_{ij,n} - S^{Ref_w}_{ij,n}\right| \quad (2)$$

Where S^{Ref} is the S-parameter associated to the reference data, with k associated to the load standards and w associated to the line standards, $S^{k}ij_{,n}$ is the nth s-parameter measured with $n \in [1 \div 2]$ being the considered error set, and $i,j \in [1,2]$.

The results of this comparison are two synthetic figures of merit, comprehensive of all the performed measurements, summarizing the error committed by employing a specific calibration technique, and are shown in Fig. 4. When measuring transmission lines (see, Fig. 4a, full squares for fused silica calibration, asterisks for ISS calibration), where the sources of error are dominated by the probe displacement on the transmission lines that are not accounted for by the simulations, both errors tend to increase with frequency. However, fused silica based calibration performs better than ISS in the entire frequency range, with an error 2,5 times smaller at 50 GHz. When the one port measurements are considered, probe displacement error has very small impact on the calibration accuracy [10]. In this case, the error will be mainly determined by the accuracy of the standard definition. As shown in Fig. 4b, while the error associated to the calibration on fused silica is constant versus frequency, the error associated to the conventional ISS calibration is frequency dependent and results to be always higher than the error committed when measuring with the method proposed in this paper (see, Fig. 4b), with a discrepancy that can reach one order of magnitude at 50 GHz.



a)



b)

Fig. 4: Worst case error bound for a) measurements of transmission line and b) measurements of one port loads, obtained by using fused silica calibration (■) and ISS calibration (*).

Additional insight can be obtained by considering the impedances of the loads as measured with the two calibrations, as shown in Fig. 5. To exemplify the problem, we focus on the measurements of a very low impedance load, featuring a DC resistance of 0.35 Ω (see, Fig. 5, red curves) and a very high impedance load, with a DC resistance of 4500 Ω (see, Fig. 5, black curves). For the real part of the impedance, both calibrations give results close to simulations (see, Fig. 5a). However, when the imaginary part of the impedance is considered, the ISS calibration is only valid at very low frequencies, while fails to predict the correct values as the frequency increases (see, Fig. 5b). Particularly interesting is the measurement of the very high impedance load, where the ISS calibration shows a positive value for the imaginary part of the impedance, totally neglecting the mainly capacitive behavior of the DUT, which instead is accounted for by the fused silica calibration. This behavior can be easily associated to the inaccurate inductive model of the ISS load, as also described in [10].

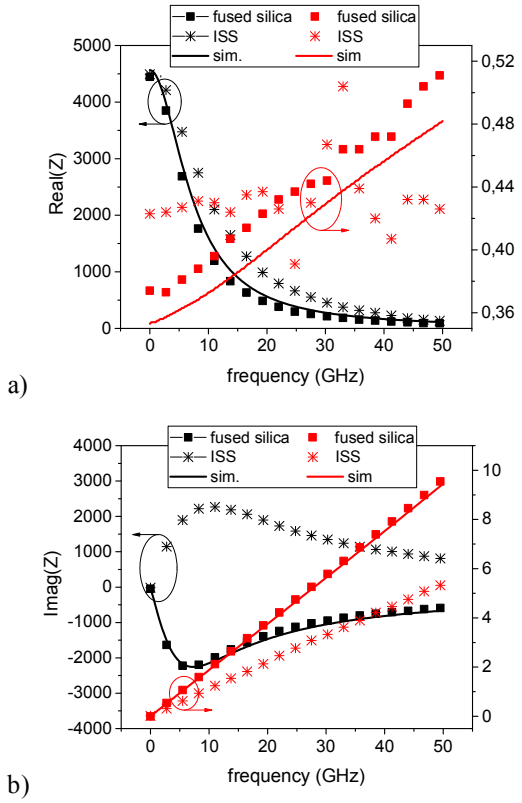


Fig. 5: a) Real and b) Imaginary part of the impedance extracted from the measurements of a 4500 Ω (black curves and symbols) and a 0.35 Ω (red curves and symbols) obtained by using fused silica calibration (■) and ISS calibration (*) as compared to simulations (solid lines).

V. Conclusions

In this paper, we presented the implementation of an RSOL calibration substrate manufactured on fused silica using integrated circuit technology. The high accuracy of the manufacturing process allows avoiding laser trimming for the definition of load standard DC resistance. When used in combination with EM simulation based calibration standard models, this calibration kit allows to avoid non-physical behaviors in s-parameter and impedance measurements while also improving measurement accuracy in respect to calibration kits provided with lumped probe-paired calibration standard definitions.

Acknowledgement

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