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Improved RSOL Planar Calibration via EM Modelling and Reduced Spread Resistive Layers

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***Abstract* — In this contribution we analyze the accuracy improvements of Reciprocal SOL planar calibrations when employing full-wave EM simulation to extract the standard's models. The calibration accuracy is benchmarked with the conventional (polynomial fit) standard definitions as well as with calibration techniques employing standards with partially-unknown parameters, as the LRM.**

Moreover, an outlook at a technology based on integrated circuit fabrication, employing fused silica substrates is described in terms of the achievable spread of its conductive and resistive layers. Such technology, in combination with the proposed EM modelling of the standards would allow to reduce the residual errors of planar calibrations.

***Index Terms* — VNA, calibration, on-wafer, EM simulation, fused silica.**

I. Introduction

The accuracy of a vector network analyzer (VNA) calibration is directly related to the knowledge of the standards employed in the procedure. Traditionally, calibration techniques requiring little standards knowledge (e.g., TRL, LRL, LRM) have been considered the most accurate, with TRL reaching metrology institute precision, by only requiring the information of the characteristic impedance of the line [1].

Nevertheless, when moving to on-wafer environments and requiring a broad-band frequency range of the calibration, the usability of TRL is limited. This is due to the large number of lines required by multi-line TRL [2], which occupy a large chip/substrate area and impose large probe movements, due to the different lines lengths.

More space efficient calibration procedures, such as the LRM [3], suffer from a non-reactive load in its original definition. Imposing partial or full knowledge of some standards allows to extract or incorporate a reactive behavior in the match load, as done in the LRRM [4] and LRM+ [5].

Nevertheless, as the TRL also the LRM technique sets the calibration reference plane in the middle of the (non-zero) coplanar thru line, thus requiring an accurate model of the thru to shift the reference plane back to the probe tips.

When coupled with accurate standard models, the reciprocal SOL (RSOL) using an unknown thru [6] can provide accuracy levels comparable to those of the TRL technique [7][8] directly setting the reference plane at the probe tips. Moreover, the lumped nature of the employed standards, when compared to TRL/LRM techniques, makes some of the standards employed in the RSOL less sensitive to probe displacement. Up to date only simple, purely reactive models are provided with commercially available calibration kits, due to the required compatibility with old firmware analyzers.

In [7] accurate frequency dependent models were acquired employing a measurement procedure, thus requiring a first-tier accurate calibration to be performed.

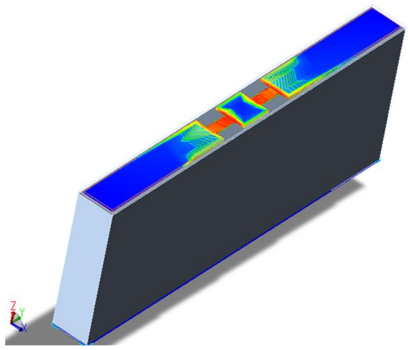

Fig. 1: 3D model of match load after Momentum simulation, indicating field intensity over the conductor and resistive layer surfaces.

In this contribution we propose the use of full wave EM simulations to extract the standard's behavior, thus increasing the accuracy of the calibration without increasing the complexity or number of measurements.

The paper is structured as follows, first the EM model generation is described and benchmarked against the conventional standard definitions using an experimental one-port calibration. After, we analyze the error propagation due to probe misplacement for the RSOL and LRM calibration, using a measurement based simulation environment coupled with electro-magnetic models for the planar standards. Finally, a technology outlook on next generation calibration standards implemented using integrated circuit manufacturing techniques on fused silica is given. The accurate control (vertical) of the conductive and resistive layers is presented by means of their resistivity uniformity over a 4 inch wafer.

Moreover the height control of thin wafers and the suppression of possible roughness arising from the carrier substrate is presented using TEM images.

II. EM Modelling of The Standards

In order to accurately extract the frequency response of the standards, a precise measurement of the dimension was performed using a Dektak 8 profilometer with a few nanometer of vertical resolution together with an optical analysis with a reference scale.

The standards composing a Cascade Microtech ISS model 101-190C were then drawn and simulated in a 2.5D full-wave EM environment (i.e., Keysight Momentum), as shown in Fig. 1. As was mentioned in [8], the short and open standard are fundamentally determined by their inductive and capacitive behavior, respectively, as also included in the simple polynomial fitting approach provided by the manufacturer of commercial kits. Nevertheless, the absence of the (small) conductive losses makes the models inaccurate and often leading to non-physical s-parameters, i.e., reflective standard providing $|\Gamma|>1$.

The largest difference between the model provided by the manufacturer and the EM simulated one is observed on the load standard, see Fig. 2. Here is clearly seen that the pure inductive model of the load is inaccurate, since the large capacitive loading provided by the contacting metal stripes is neglected or under estimated when included as a negative inductance [4].

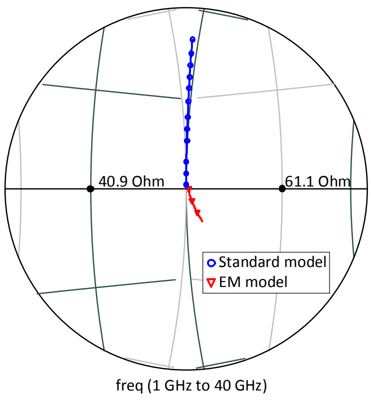

Fig. 2: Zoom-in of Smith chart presenting the standard model from the kit manufacturer and the EM extracted model for the load resistor.

A. Experimental benchmarking of commercial standards

In order to evaluate the impact of the new standard definitions (derived from the EM simulations) various one-port measurements were performed.

When analyzing data from the open termination, while no information of the accuracy can be derived, being the SOL a fully known calibration, it is evident from Fig. 3 that only a definition of the standard including losses (right), avoids the generation of non-physical s-parameter data (left).

The improved accuracy achieved when using EM simulations for the standards definition can be better quantified using a worst case bound metric. Here, two calibration were performed on the same set of measurements using the classical models (std.) and the proposed ones (EM).

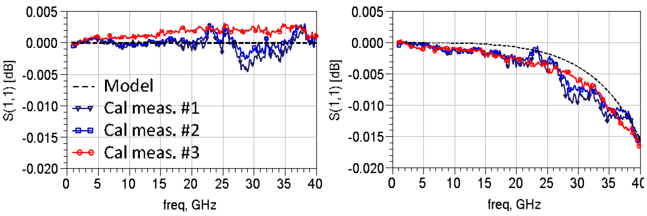

Fig. 3: Measurement versus model of the open standard: (left) employing standard model definitions, (right) employing EM extracted model definition for the calibration.

After, three raw measurements where performed on different samples of a 220um 50 Ohm line, with port two left open and the two calibration terms where applied to the same data. All the data acquisition, generation of the calibration terms and data correction was performed using Cascade Microetch Wincal XE ver. 4.5 [9].

In order to compare the different calibrations, the method of [10] has been adapted to a one port-calibration , defining an error metric (for the standard and the EM calibration) as:

$$WCB = \max\left|S'_{11,n} - S_{11}\right| \tag{1}$$

Where S_{11} is the s-parameter associated to the reference data (i.e., simulation of the open-ended thru line), and $S'_{11,n}$ is the nth s-parameter measured with $n \in [1,2,3]$.

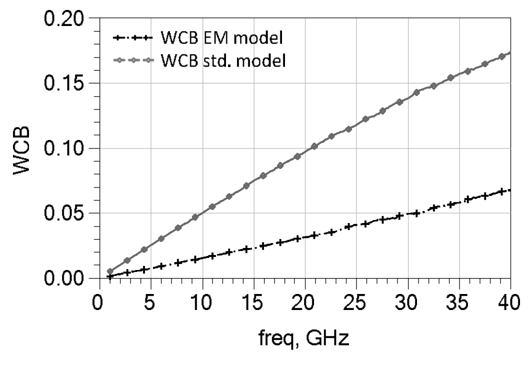

Fig. 4: Worst case error bound (WCB) as computed from equation 1, among three calibrated measurement employing the standard models (○) and the EM derived models (+).

Fig. 4 indicates how the WCB for the calibration using EM simulated standards is well below the value achieved by the conventional standard definitions.

III. MEASUREMENT BASED SIMULATION ENVIRONMENT

When considering two-port s-parameter measurements we can opt for different calibration algorithms, which impose diverse requirements on the standard's knowledge. In order to evaluate the differences in uncertainty and accuracy, with the constraints of on-wafer calibration, we need to propagate the errors caused by probe misplacement through the various calibration algorithms. For this purpose a simulation environment was created in the Keysight ADS environment as described in [11], see Fig. 5.

To correlate the simulation environment to the experimental setup, a calibration was first performed on the VNA in the frequency band of interest, including probes and cables as will be used in the final experimental analysis. The input and output error-terms (e_d, e_s and e_t) were extracted from the VNA and converted in a two port data item imposing $S21=e_t$ and $S12=1$. Using this approach, when performing a calibration in the simulation environment, the computed error-terms will be exactly the one of the considered measurement setup.

At this point the calibration standards created in the Momentum EM environment (see section II) are converted in a parametric model, where the variable is the offset of the EM port to the nominal position, see Fig. 6.

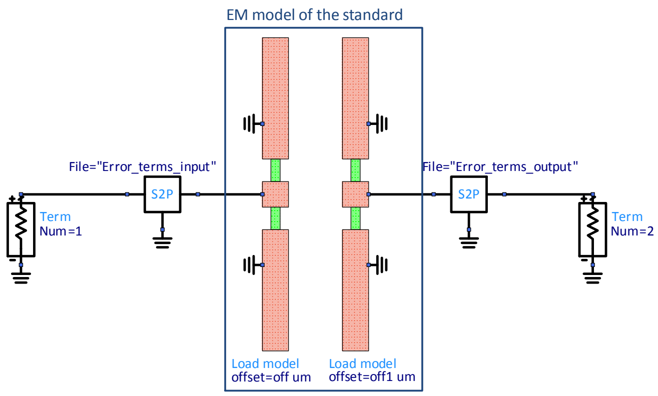

Fig. 5: Block diagram of measurement system, using experimental setup error model, implemented in Keysight's Advanced Design System (ADS) software.

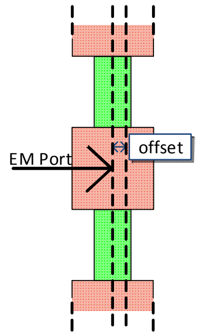

Fig. 6: Offset variable in parametric EM models used to propagate probe misplacement through different calibration algorithms.

The calibration techniques compared by the proposed simulation approach were the RSOL and LRM technique. The first technique requires full knowledge of the one-port standards (SOL) while only requiring passivity from the two-port connection. The LRM technique, in its original form, requires full knowledge of the two-port standard (i.e. thru), a known resistive behavior from the match termination, and only the phase quadrant information of the reflect (i.e., knowledge if it has an open or short behavior). Moreover the LRM technique employs one standard less than the RSOL. A Montecarlo simulation (employing 101 iterations) is then performed on two independent uniformly distributed variables representing the EM port position (i.e., mapping the probe misplacement at port one and two) of ±7.5μm.

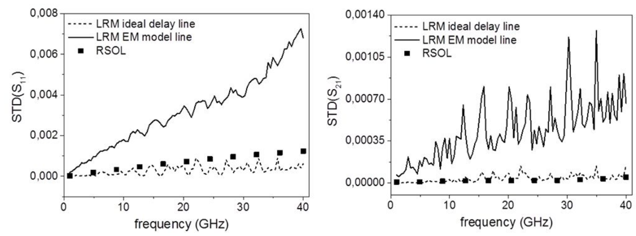

Fig. 7: Standard deviation computed from the Montecarlo simulation, for the magnitude of the reflection (left) and transmission (right) parameter for: the RSOL calibration (full squares), the LRM one employing an ideal delay line (dashed) or the realistic EM simulated line (solid).

After the simulation the standard deviation versus frequency is computed for the RSOL and LRM calibration. When employing a realistic thru line (with small mismatch and fluctuation in the group delay) it can be seen that the LRM technique results in a large standard deviation (i.e., propagated uncertainty from the probe misplacement) for both reflection and transmission terms, Fig. 7 left and right, respectively. Only when the thru line is replaced with an ideal delay line (i.e., no mismatch and delay fluctuation) does the LRM present an uncertainty comparable to the RSOL. Note, that this indicates that an accurate model of the thru line is required to properly apply the LRM calibration, which is in contrast to the simple data available from the calibration substrate definitions.

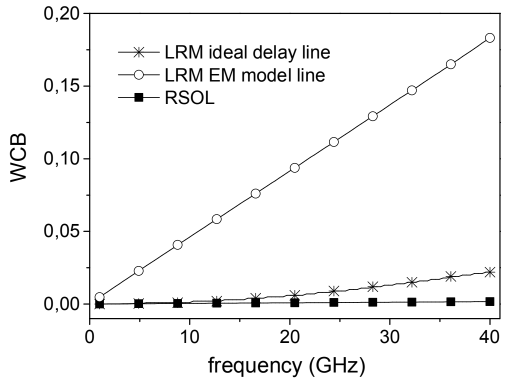

Fig. 8: Worst case error bound computed as in [10] from simulated data using as a 450µm verification device line and employing the EM simulation of the line as the reference for the metric computation.

When computing the WCB (computed using the mean value of the S parameters, as obtained from the Montecarlo simulation) as described in [10] we see a similar trend as seen for the uncertainty, with the LRM using the EM simulated data presenting the largest error. Note, that even when we employ an ideal delay line, the non-zero WCB is due to the reactive component of the load, which is not properly accounted by the standard LRM. As mentioned in section I, by providing more knowledge on the standards (i.e., model of the reflect or non-ideal load behavior) the error bound of the LRM can be reduced, when doing so, the reduced standard requirements of the technique are traded away. It is important also to mention that the error bound of the RSOL only represents a best case scenario, since within the simulation environment there is no discrepancy between the knowledge of the standards and the standards itself, this is obviously not the case for real devices.

IV. Two-Port Experimental data

In order to validate the simulation findings of section III, two-ports measurements were conducted on a Cascade Microtech ISS model 101-190C. A unique set of raw data of the standards was employed to derive the error-terms for the RSOL, employing manufacturer and EM definitions, and the LRM calibration. All the data acquisition, generation of the calibration terms, and data correction was performed using Cascade Microetch Wincal XE ver. 4.5 [9].

A raw measurement of a 450µm line present on the same calibration substrate was used to compare the data obtained applying the three set of error terms mentioned above and compute a WCB. As done for the error computed in Fig. 8 also here the EM simulation of the 450µm line was used as reference data. The WCB is shown in Fig. 9, indicating a similar behavior for the LRM as expected from simulation. The RSOL employing standards definition through EM simulations provides an improvement in the error bound, compared to the conventional definition, confirming the findings of section II.

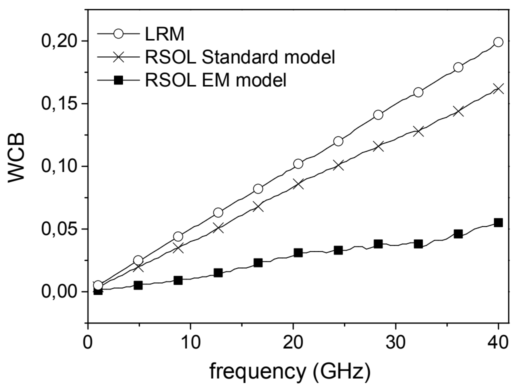

Fig. 9: Worst case error bound computed as in [10] from experimental data, using 450µm line as a verification device and employing the EM simulation of the line as the reference for the metric computation.

In general it can be stated that the WCB presented in Fig. 9 will depend strongly on the position placement accuracy for the LRM, and on the consistency of the model with the artifact for the RSOL. For this reason, the RSOL trades off complexity in the probing environment (i.e., motorized manipulators) for higher quality standards.

V. Fabrication Technology

As it has been discusses in the previous sections in order to achieve accurate on-wafer calibration the manufacturing quality of the standards needs to be improved.

In [8] it was shown that the variation of the load resistance is one of the biggest sources of uncertainty in planar SOL type calibrations. When accurate models of the standards are employed it becomes crucial to fabricate these standards and especially the load with as little variation as possible. In this section we present some preliminary results of the performance achieved by employing integrated circuits processing techniques to manufacture the calibration standards. The aimed process is based on a fused silica substrate with a simple layer stack of a resistive nitride layer and a conductive aluminum layer as sketched in Fig. 10.

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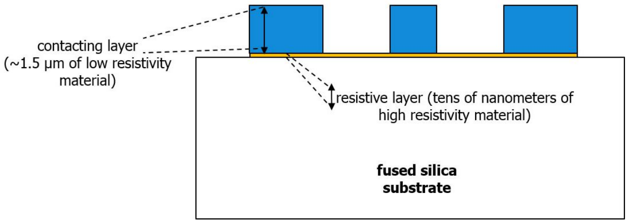

Fig. 10: Schematic cross-section of the 50 Ohm resistors fabricated on fused silica substrate.

First analysis of the uniformity of the conductive layer, measured using a 4-probe resistance measurement over the entire 4 inch wafer, show a σ variation close to 1.2%. This leads to a variation within the 2x2 mm^2 calibration die smaller than 1%, see Fig. 11.

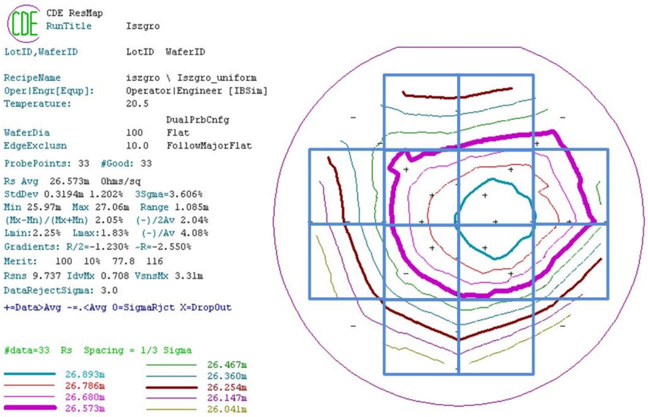

Fig. 11: Resistivity contour map over the 4 inch wafer, superimposed by the grid of 2x2 mm^2 dies. Measured standard deviation over 33 points over the entire wafer is 1.202%.

Similar measurement performed on the resistive layer show within the die a standard deviation just above 1%. The target for the process optimization is a variation below 0.5% within the die, which would allow to remove the process of laser trimming of the resistors.

Preliminary test on the conductive layer show an absorption of any substrate layer roughness by the aluminum layer already from 200nm, see Fig. 12. The targeted substrate (i.e., fused silica) will provide extremely flat polished surface, indicating that the layer roughness should be negligible.

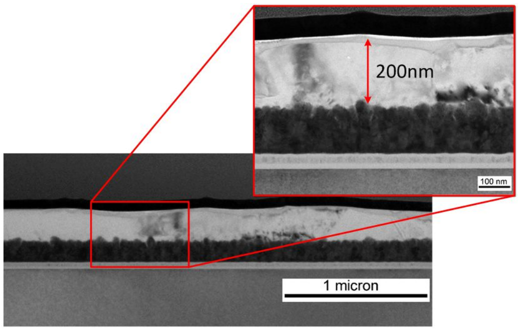

Fig. 12: TEM image of 200nm aluminum layer sputtered over a rough surface. As it can be seen by the inset the roughness is already absorbed after 200nm.

Finally, the tests conducted on the thin resistive layer, show a very good control of the layer thickness for the targeted 80 nm resistance. Moreover, the aluminum to nitride interface shows no presence of grains or defects.

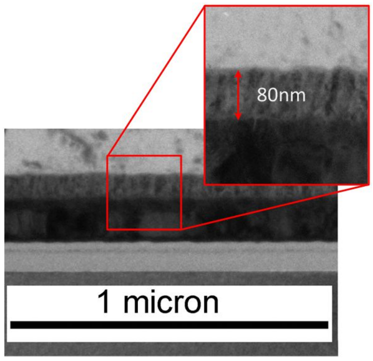

Fig. 13: TEM image of the resistive layer targeted to 80nm thickness.

VI. Conclusions

In this paper we presented the accuracy improvement which can be obtained employing full wave EM simulations to generate the planar calibration standard definitions. In both one-port and two-port experimental verification the usage of the improved standard definitions allowed to avoid non-physical s-parameter behavior and a reduced worst case error bound. Moreover, the error propagation due to probe misplacement was analyzed in a simulation environment to compare RSOL and standard LRM calibrations. The insensitivity of the RSOL to the probe misplacement of the thru device led, in conjunction with the improved standard definitions, to a reduced worst case error bound. Experimental data was presented confirming the simulation analysis. Finally, and outlook of a technology to potentially improve the manufacturing quality of the standards was briefly discussed.

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